

CLAIMS

What is claimed is:

1. A process for fabrication of a semiconductor device comprising a non-volatile memory cell having a modified ONO structure, comprising forming the modified
5 ONO structure by steps comprising:

providing a semiconductor substrate;

forming a first oxide layer on the semiconductor substrate;

depositing a layer comprising a high-K dielectric material on the first oxide layer;

and

10 forming a top oxide layer on the layer comprising a high-K dielectric material.

2. The process of claim 1, wherein the semiconductor device comprises a two-bit EEPROM device or a floating gate flash device.

15 3. The process of claim 1, wherein the step of depositing a layer comprising a high-K dielectric material is carried out by ALCVD or MOCVD.

4. The process of claim 1, wherein the steps of forming an oxide layer, depositing a layer comprising a high-K dielectric material and forming a top oxide layer are
20 carried out in an RTP and RTCVD apparatus.

5. The process of claim 1, wherein the steps of forming an oxide layer, depositing a layer comprising a high-K dielectric material and forming a top oxide layer are carried out in a single-wafer cluster tool.
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6. The process of claim 1, wherein the layer comprising a high-K dielectric material is deposited to a thickness of about 50 to about 300 angstroms.

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7. The process of claim 1, wherein the high-K dielectric material comprises at least one of hafnium oxide (HfO_2), zirconium oxide (ZrO_2), tantalum oxide (Ta_2O_5), barium titanate (BaTiO_3), titanium dioxide (TiO_2), cerium oxide (CeO_2), lanthanum oxide (La_2O_3), lanthanum aluminum oxide (LaAlO_3), lead titanate (PbTiO_3), strontium titanate (SrTiO_3),
5 lead zirconate (PbZrO_3), tungsten oxide (WO_3), yttrium oxide (Y_2O_3), bismuth silicon oxide ($\text{Bi}_4\text{Si}_2\text{O}_{12}$), barium strontium titanate (BST) ($\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$), PMN ($\text{PbMg}_x\text{Nb}_{1-x}\text{O}_3$), PZT ($\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$), PZN ($\text{PbZn}_x\text{Nb}_{1-x}\text{O}_3$), and PST ($\text{PbSc}_x\text{Ta}_{1-x}\text{O}_3$).

8. A process for fabrication of a semiconductor device, the device including a
10 two-bit EEPROM device including a modified ONO structure, comprising forming the modified ONO structure by steps comprising:

providing a semiconductor substrate;

forming a tunnel oxide layer overlying the semiconductor substrate;

15 depositing a layer comprising a high-K dielectric material overlying the tunnel oxide layer; and

forming a top oxide layer overlying the layer comprising a high-K dielectric material.

9. The process of claim 8, wherein the steps of forming a tunnel oxide layer, depositing a layer comprising a high-K dielectric material and forming a top oxide layer are
20 carried out in an RTP apparatus which is a component of a single-wafer cluster tool.

10. The process of claim 8, wherein the step of depositing a layer comprising a high-K dielectric material is carried out by ALCVD or MOCVD.

25 11. A process for fabrication of a semiconductor device, the device including a floating gate flash structure comprising a modified ONO structure, comprising forming the modified ONO structure by steps comprising:

providing a semiconductor substrate having a floating gate electrode overlying a tunnel oxide;

30 forming a bottom oxide layer overlying the floating gate electrode;

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depositing a layer comprising a high-K dielectric material overlying the bottom oxide layer; and

forming a top oxide layer overlying the layer comprising a high-K dielectric material.

5 12. The process of claim 11, wherein the steps of forming a bottom oxide layer, depositing a layer comprising a high-K dielectric material and forming a top oxide layer are carried out in an RTP apparatus which is a component of a single-wafer cluster tool.

10 13. The process of claim 11, wherein the step of depositing a layer comprising a high-K dielectric material is carried out by ALCVD or MOCVD.

15 14. The process of claim 11, with the proviso that when the layer comprising a high-K dielectric material comprises tantalum oxide (Ta_2O_5), it further comprises at least one additional dielectric material.

 15. The process of claim 1, wherein the layer comprising a high-K dielectric material further comprises a second dielectric material.

20 16. The process of claim 1, wherein in the layer comprising a high-K dielectric material, the high-K dielectric material is sandwiched between layers of a nitride.

25 17. The process of claim 1, wherein in the layer comprising a high-K dielectric material, a second dielectric material is combined with at least a portion of the high-K dielectric material to form a composite dielectric material.

 18. The process of claim 17, wherein the composite dielectric material is formed by depositing alternating sub-layers of each dielectric material.

30 19. The process of claim 17, wherein the composite dielectric material is formed by simultaneously depositing each dielectric material.

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20. The process of claim 1, wherein the top oxide layer is formed on the layer comprising a high-K dielectric material in the absence of exposure of the high-K dielectric material to ambient atmosphere prior to formation thereon of the top oxide layer.